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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,234	07/22/2003	Kentaro Tani	299002056700	8620
25226	7590	03/28/2005	EXAMINER	
MORRISON & FOERSTER LLP 755 PAGE MILL RD PALO ALTO, CA 94304-1018				SEFER, AHMED N
		ART UNIT		PAPER NUMBER
		2826		

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,234	TANI, KENTARO	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 05 January 2005.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
 4a) Of the above claim(s) 5-20 is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-4 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

Election/Restrictions

1. Newly submitted claims 9-20 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: A materially different process that does not include a step of washing the first stacked semiconductor structure and the striped ridge structure with a washing liquid could make the device of claim 1.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 9-20 have been withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Drawings

2. Figures 5A-5D should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled “Replacement Sheet” in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (APA).

The APA discloses in figs. 5A-5D a semiconductor light emitting device, comprising: a semiconductor substrate; a stacked semiconductor structure formed on the semiconductor substrate; a striped ridge structure; and a semiconductor current confinement layer 111 provided on a side surface of the striped ridge structure; wherein the stacked semiconductor structure includes a first semiconductor clad layer 103, a semiconductor active layer 104, a second semiconductor clad layer 105, and a semiconductor etching stop layer 106; wherein the striped ridge structure includes a third semiconductor clad layer 107, a semiconductor intermediate layer 108, and a semiconductor cap layer 109; wherein the striped ridge structure is provided on the semiconductor etching stop layer; wherein an interface between the semiconductor current confinement layer and the semiconductor etching stop layer and an interface between the semiconductor current confinement layer and the striped ridge structure each having impurities and wherein the impurities are carbon/oxygen based (as in claims 2-4), but lacks anticipation of an impurity concentration. However, it would have been obvious to meet the recited impurity concentration since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art.

In re Aller, 105 USPQ 233.

5. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsunoda JP 2001-196694.

Tsunoda discloses in fig. 1 a semiconductor light emitting device, comprising: a semiconductor substrate; a stacked semiconductor structure formed on the semiconductor substrate; a striped ridge structure; and a semiconductor current confinement layer 13 provided on a side surface of the striped ridge structure; wherein the stacked semiconductor structure includes a first semiconductor clad layer 4, a semiconductor active layer 5, a second semiconductor clad layer 6, and a semiconductor etching stop layer 7; wherein the striped ridge structure includes a third semiconductor clad layer 8, a semiconductor intermediate layer 9, and a semiconductor cap layer 10; wherein the striped ridge structure is provided on the semiconductor etching stop layer; wherein an interface between the semiconductor current confinement layer and the semiconductor etching stop layer and an interface between the semiconductor current confinement layer and the striped ridge structure each having impurities (see col. 7, lines 54-67 of equivalent reference USPN 6,518,159) and wherein the impurities are carbon/oxygen based (as in claims 2-4), but lacks anticipation of an impurity concentration. However, it would have been obvious to meet the recited impurity concentration since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art.

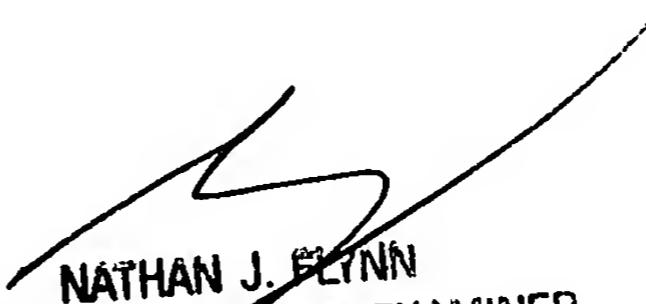
In re Aller, 105 USPQ 233.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
March 18, 2005


NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800